

Fig. 1

<u>Inst</u>	<u>Hit/Miss</u>	<u>Data</u>
18 — LDR [R _m]	Hit	Data [R _m]
MOV	N/A	—
CMP	N/A	—
⋮	⋮	⋮
20 — LDR [R _m]	Miss	—
MOV	N/A	—
CMP	N/A	Data [R _m]
⋮		
22 — LDR [R1]	Miss	—
24 — LDR [R2]	Miss	—
MOV	N/A	—
CMP	N/A	28 — Data [R2]
ADD	N/A	26 — Data [R1]

variable delay

missed data returned out of order

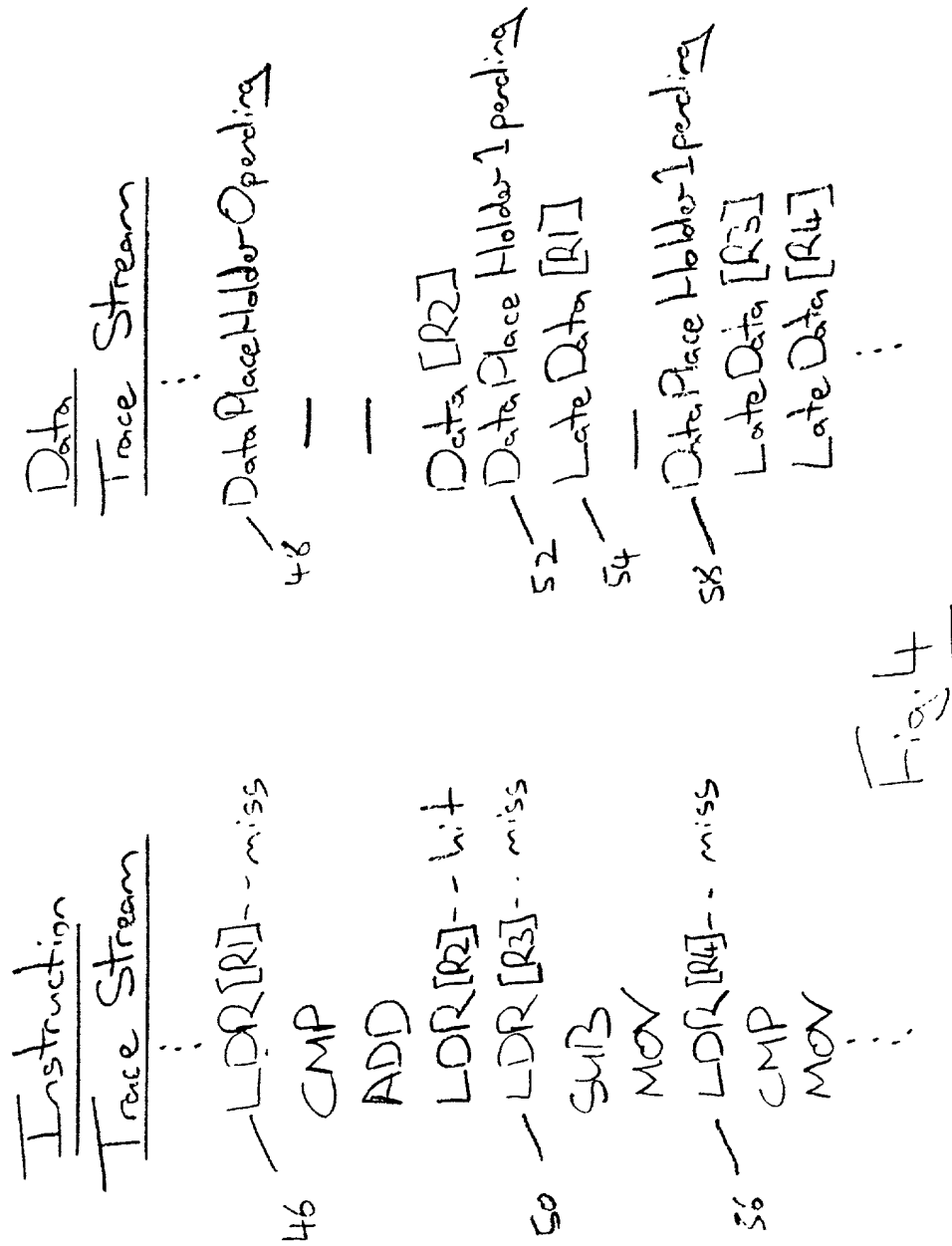


Fig. 4

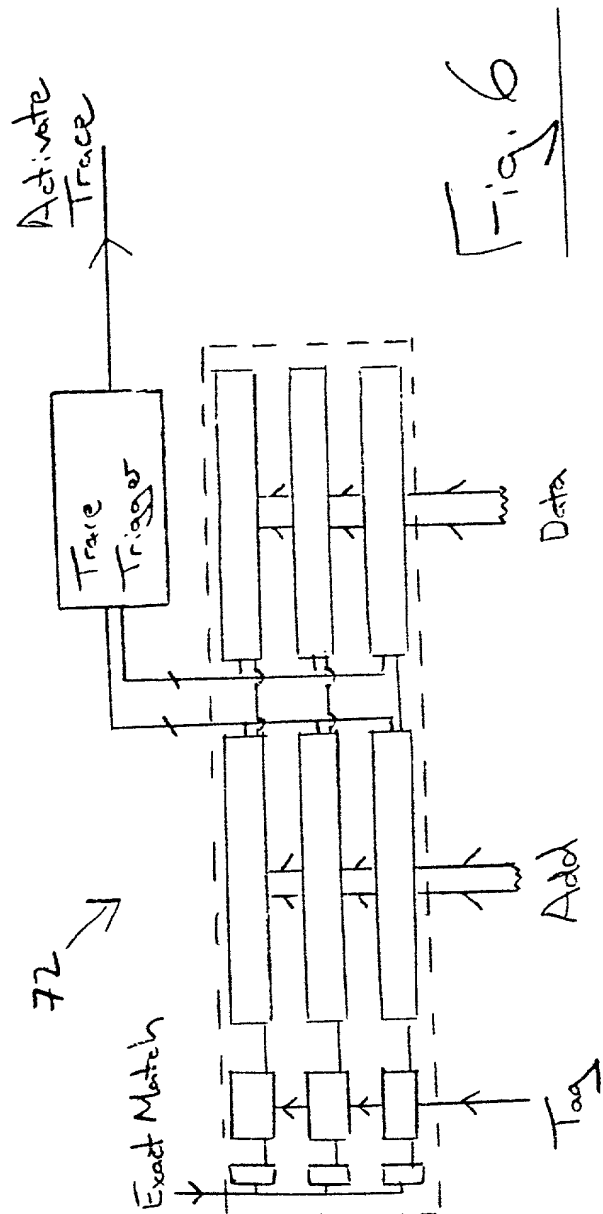


Fig. 6

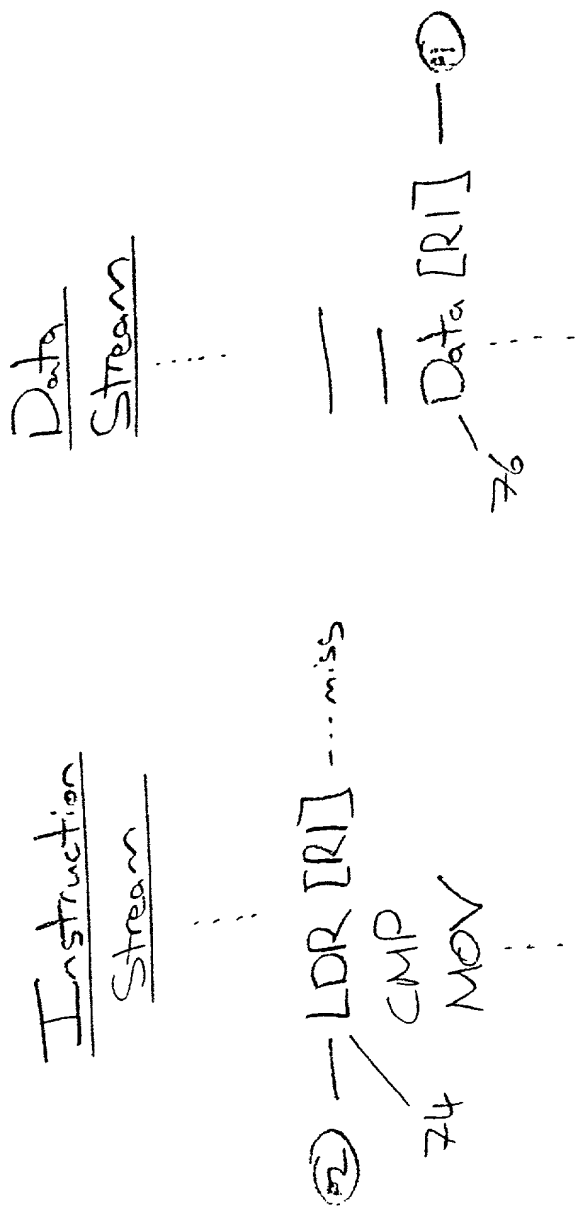


Fig. 7

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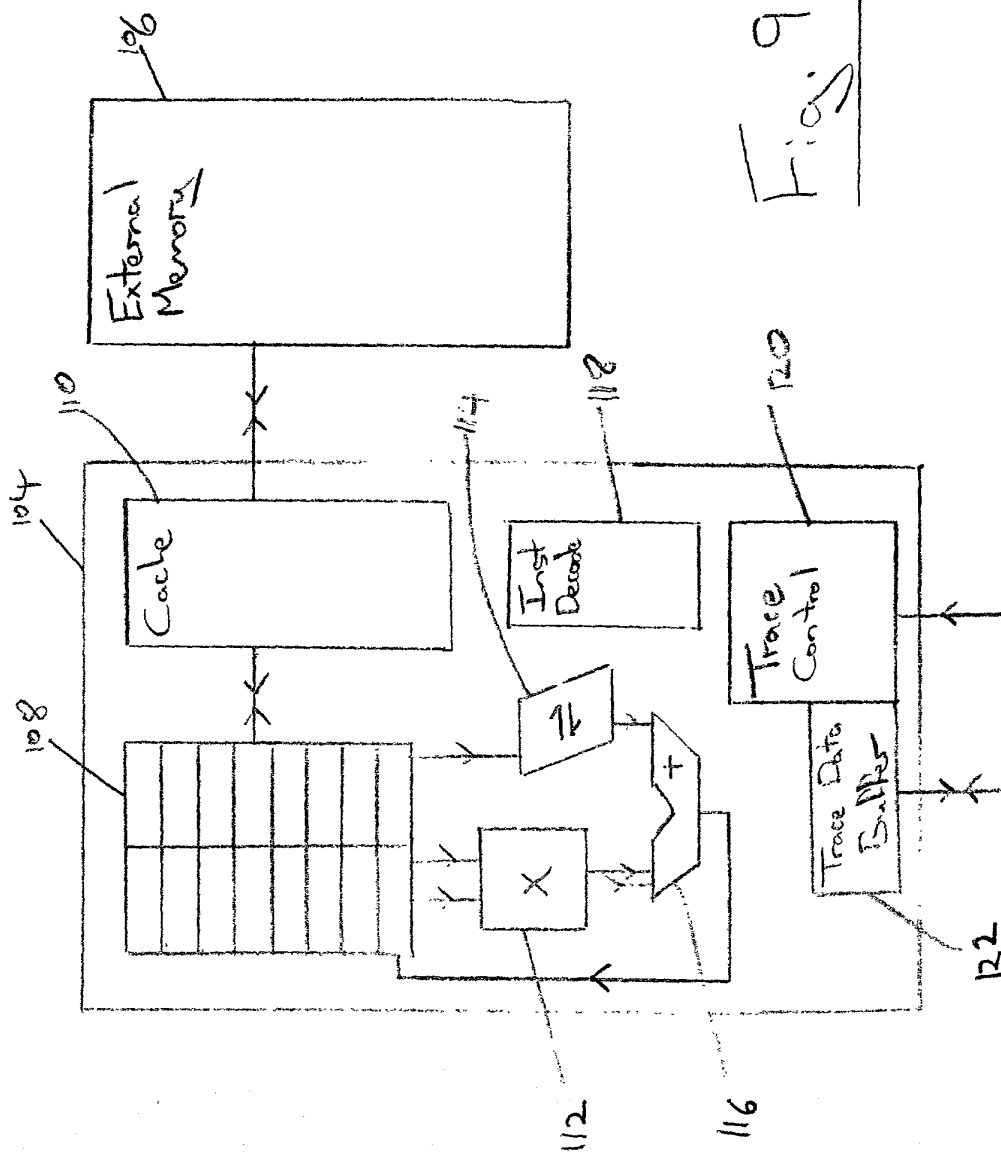


Fig. 9

LSM $R_n[Add]$, $RegList$

16 bits

0000 1000 1000 1011



R0	
R1	
R2	R11
R7	

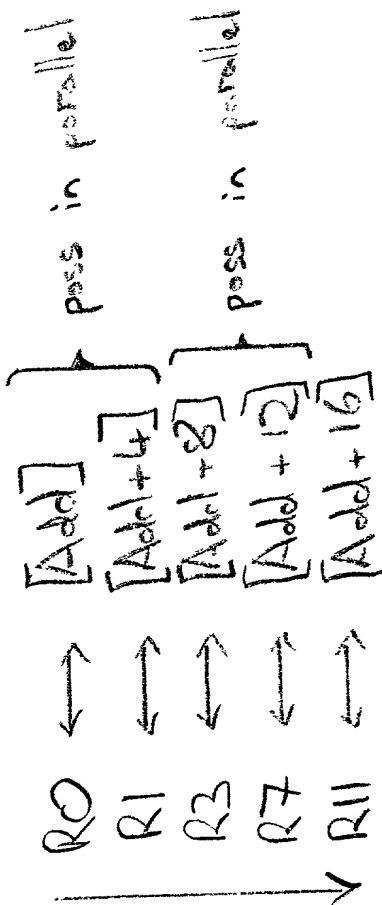
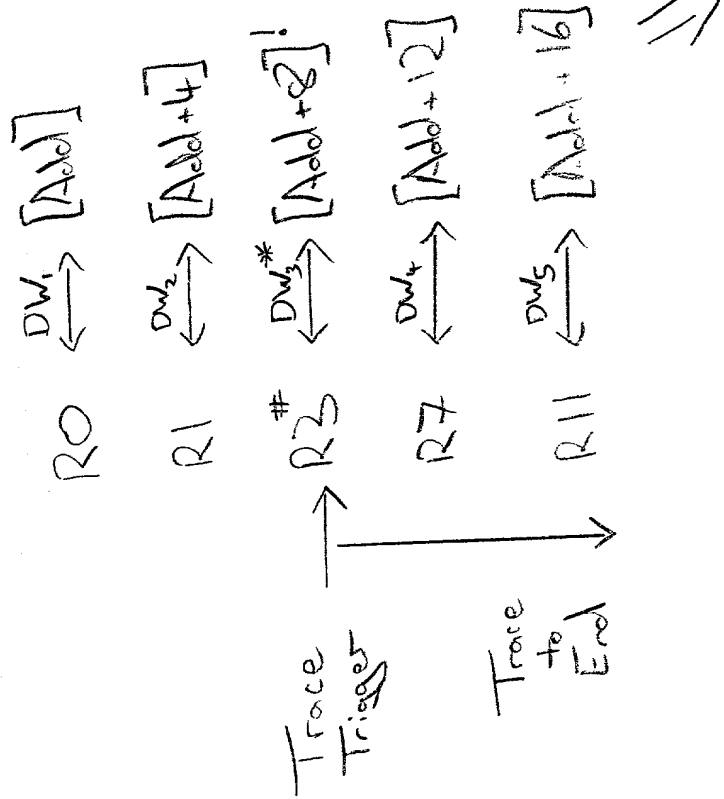


Fig. 10



Trace Data Stream

..., {LSNR}, {Addr}, {DW₃}, {DW₄}, {Place Holder}, {Place Holder}, ...

← Count back to R3

Fig. 11

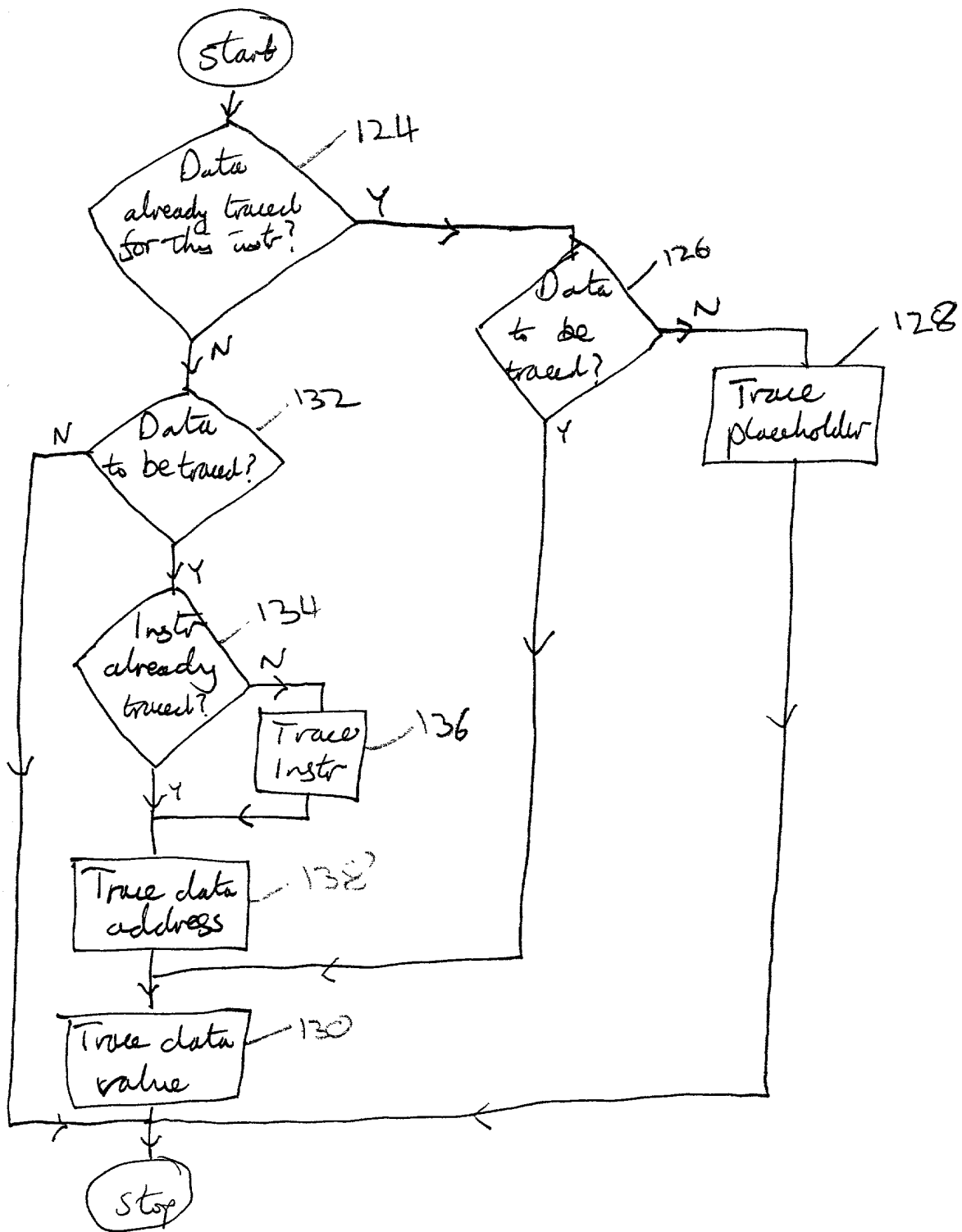


Fig. 12

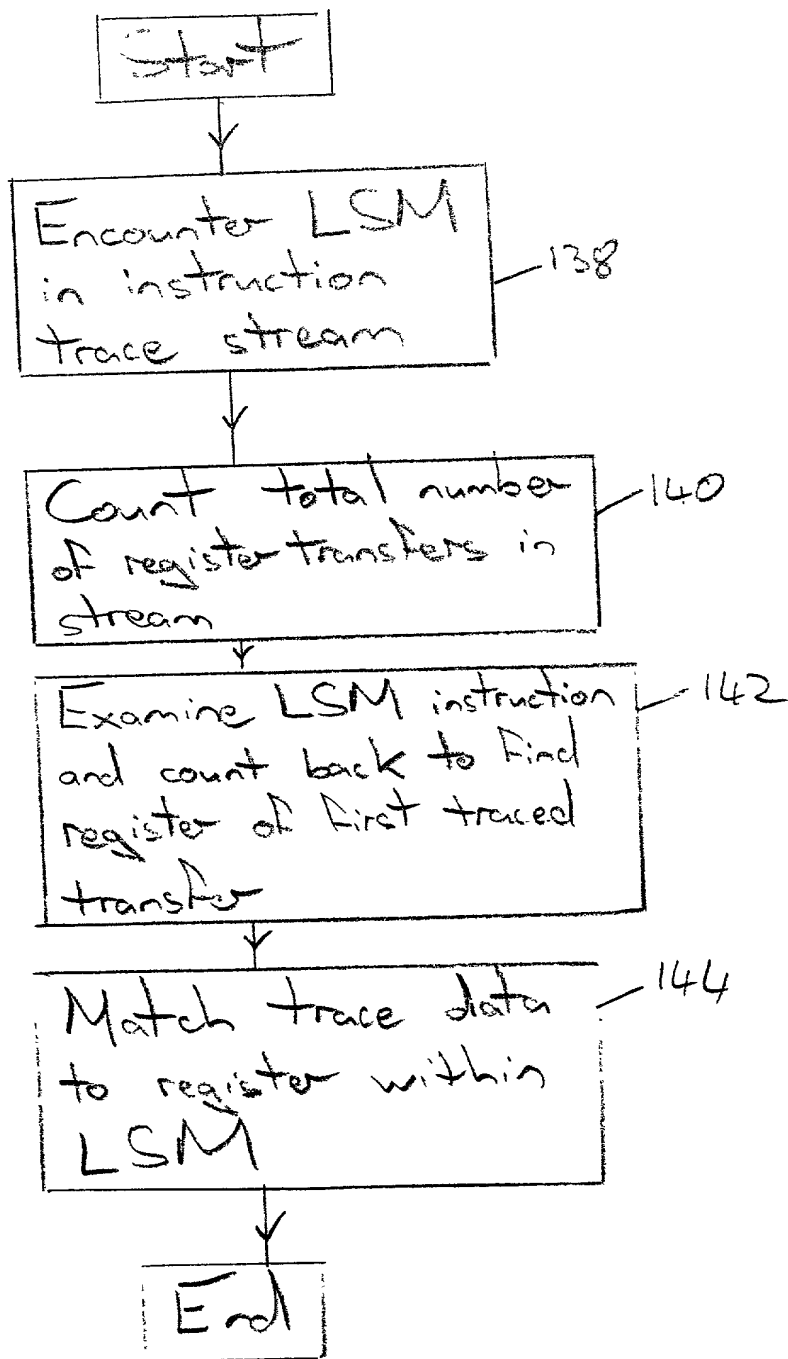


Fig. 13